

Building a modular transmitter: mixer and reference oscillator

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Abstract

I obtained my ham radio license more than twenty years ago and until recently, I had never build a radio transmitter. I will publish a series of articles about the design and build of a modular radio transmitter, using mostly discrete components. The third module I have designed is a frequency mixer and reference oscillator for the mixer itself and for the PLL.

1 An overview

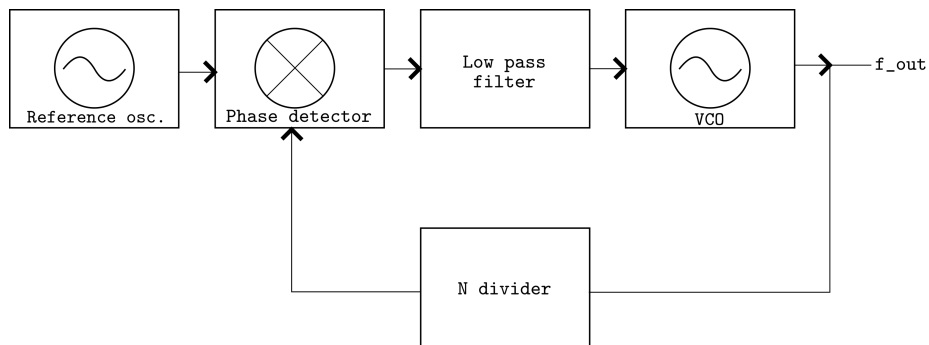


Figure 1: block diagram of the PLL

Figure 1 shows the block diagram of the PLL. The N divider can divide the input signal by 1 up to 999. For technical reasons, a pulse shaper divides the signal again by two. When set to 500, an input frequency of, say, 500 kHz comes out of the divider as a 500 Hz signal. This is the frequency at which the PLL works. The reference oscillator therefore has to be 500 Hertz as well. This PLL can synthesize frequencies from 1kHz all the way up to 999kHz. As I want to build a transmitter for the 80 meter amateur radio band, I have to convert a 3.5MHz signal to a signal somewhere in between 1kHz and 999kHz. I choose 500kHz, slap bang in the middle of the range of the programmable divider. This way I have a wide frequency range of plus and minus 500kHz for adjustment. For this conversion I cannot use another frequency divider, as it will lower the resolution of the PLL. To maintain the 1kHz step size, I have to use a mixer. In figure 2 you can see the PLL with this mixer in the feedback loop.

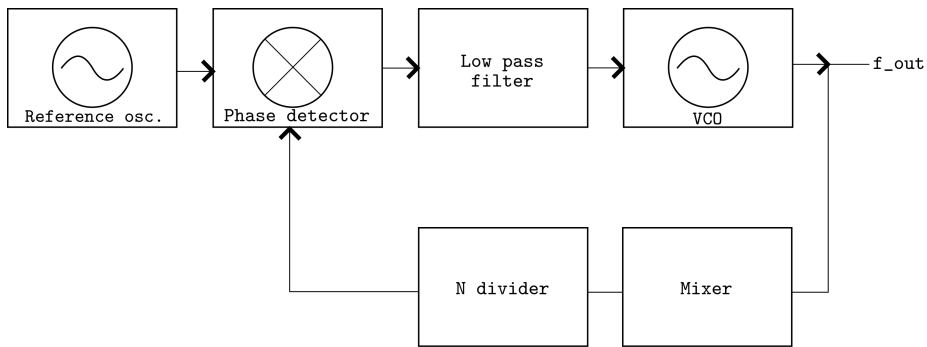


Figure 2: block diagram of the PLL with mixer

2 The mixer

2.1 The input amplifiers

Figure 3 shows the block diagram of the mixer. A mixer is often used in rf designs. It can add and subtract two frequencies. In the example you can see two input signals. A 4MHz signal and a 3.5MHz signal. The mixer adds as well as subtracts both signals, resulting in two new signals at the output: a 7.5MHz signal and a 500kHz signal. A low pass filter removes the 7.5MHz signal, leaving just the 500kHz signal, needed as input signal for the programmable divider.

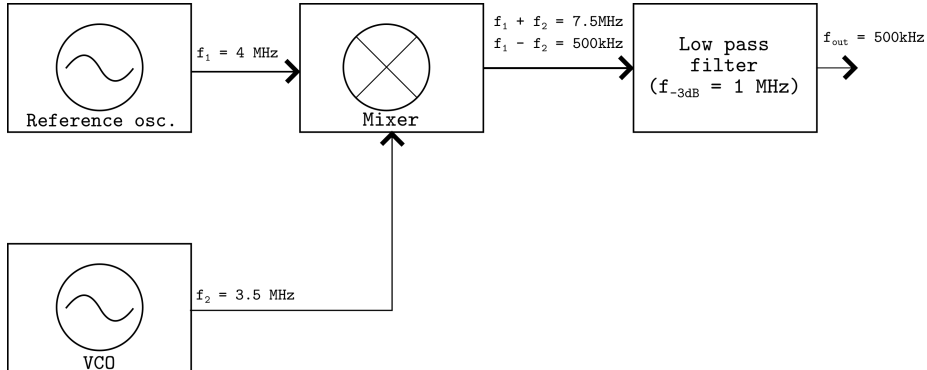


Figure 3: block diagram of the mixer

The mixer is constructed from four separate circuits, as can be seen in figure 4. First, both input signals are buffered by two isolation amplifiers. As the name suggests, these amplifiers isolate the inputs from the outputs. This prevents the mixing products from feeding back into the inputs. After that, the actual mixer and low pass filter follow.

Figure 5 shows the actual schematic of one of the input buffers. It is build around a common base amplifier. A characteristic of a common base amplifier is its low input impedance. Here about 50 Ohms. Transmission lines connected to the input are correctly terminated, preventing cable reflections. Another characteristic is the good isolation between output and input. The bandwidth

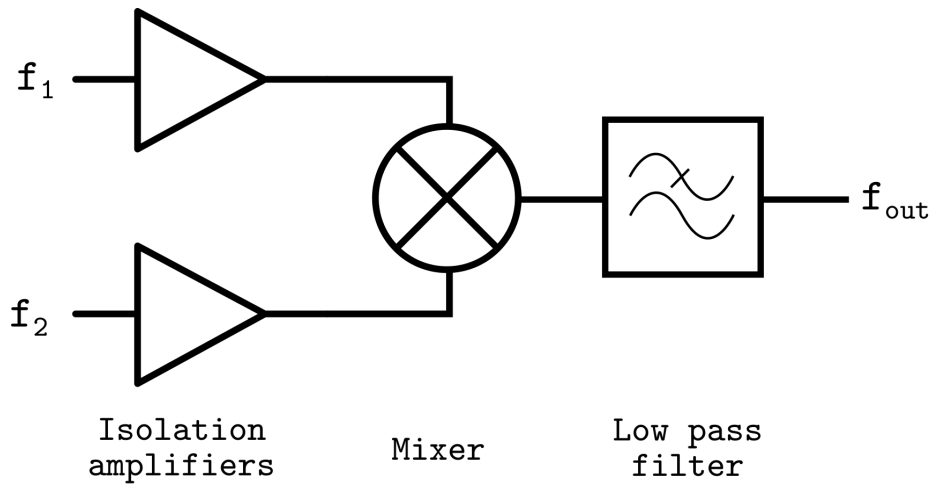


Figure 4: the mixer and its separate parts

of this amplifier is 9 MHz.

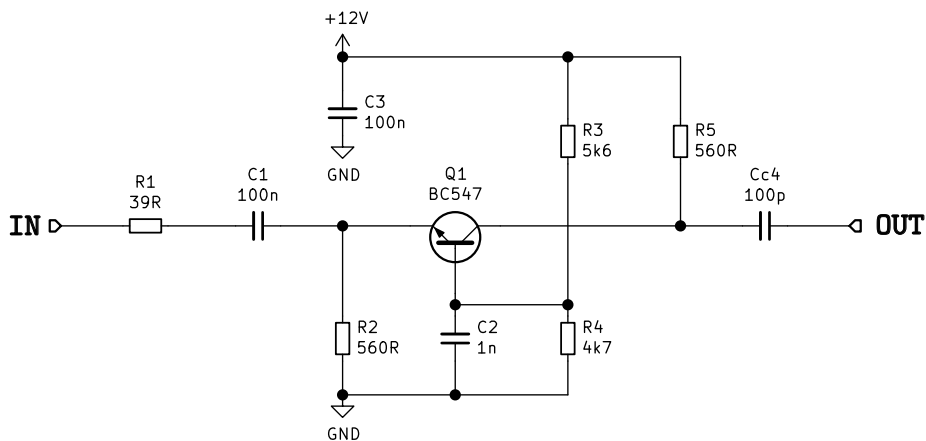


Figure 5: the input buffer, a common base amplifier

2.2 The actual mixer and low pass filter

Figure 6 shows the schematic of the mixer and low pass filter. The two signals from the isolation amplifiers (f_1 and f_2) are combined at the base of transistor Q5. This is the mixer. The low pass filter is placed directly after the mixer. Here the 7.5MHz sum frequency is filtered out leaving the difference of 500kHz in tact.

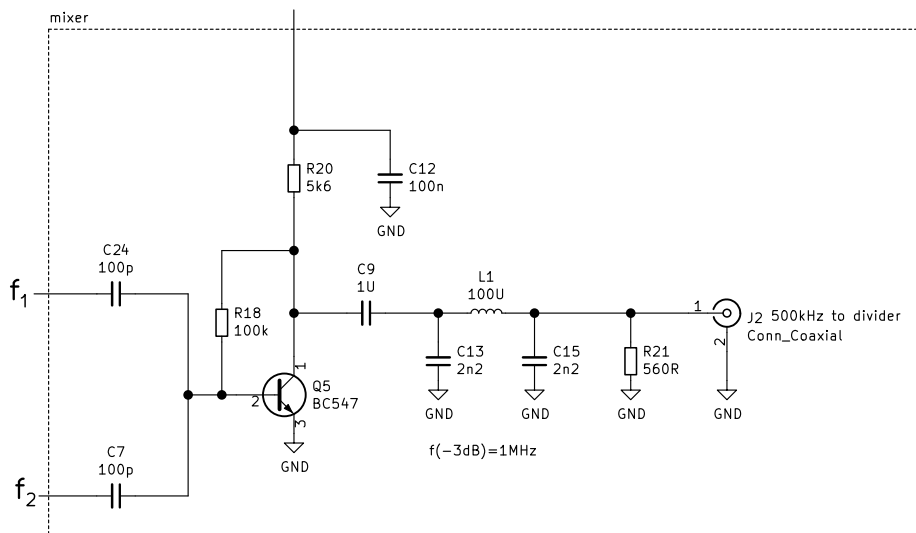


Figure 6: the mixer and low pass filter

3 The reference oscillator

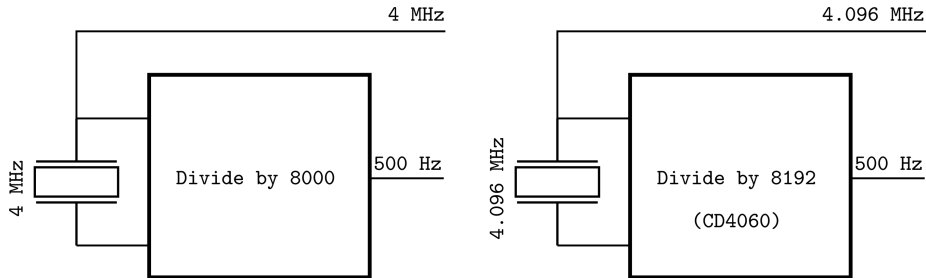


Figure 7: block diagram reference oscillator

A fixed 4 MHz reference oscillator is needed to generate a 500 kHz signal on the output of the mixer. Also, a 500Hz signal is needed as a reference for the PLL. If these signals are generated by the same oscillator than both are locked to each other. As an extra bonus, less components are needed. I can achieve this by using a 4 MHz crystal oscillator followed by a divider which divides by 8000. The programmable divider I designed for the PLL loop two can divide by 1 to 999. If I place two of these divider in series, I can divide by 1 to 9999 and thus by 8000. But thats a lot of chips! It is way easier to divide by a power of 2. Because that can be done by a bunch of flip flops. But the closest to 8000 I can get this way is 2 to the power of 13, which is 8192. A CD4060 can generate a clock and divide this clock by 8192, all in one chip. And when I use a 4.096MHz crystal instead of a 4 MHz one, dividing by 8192 gives me a 500 Hz signal. But than the main clock frequency is 4.096MHz. Lets analyze whether this is a problem:

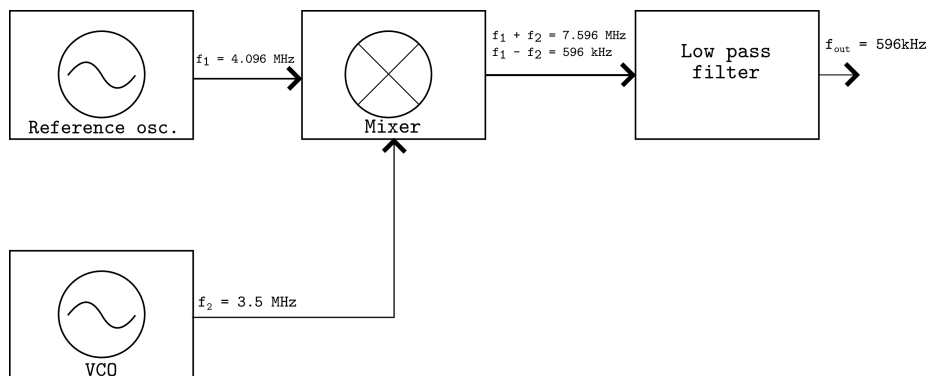


Figure 8: block diagram reference oscillator

Figure 8 shows the various frequencies when using a 4.096MHz oscillator. With the VCO at 3.5MHz, the output frequency of the mixer increases from 500kHz to 596kHz, which is still a factor of 1kHz. This means that by changing the division ratio of the programmable divider from 500 to 596 the output of this programmable divider can still be 500Hz. And the minimum frequency step remains 1kHz. Instead of a pcb full of ics I can use only the one CD4060 for

generating the two reference signals. Neat!

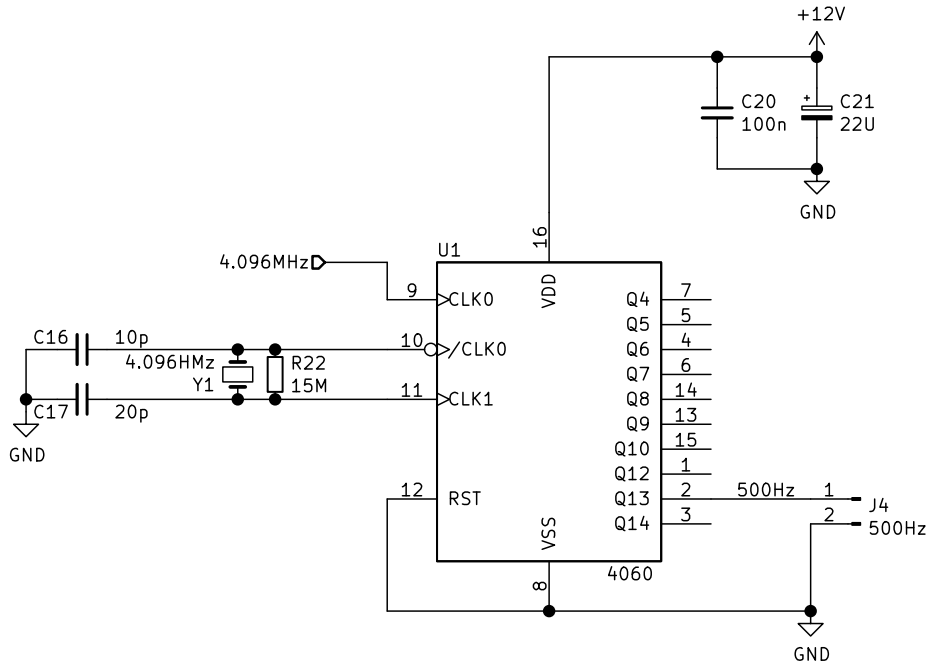


Figure 9: schematic reference oscillator

Figure 9 shows the schematic of the complete reference oscillator.

4 Bits and bobs

4.1 Attenuation and impedance matching

low impedance driver

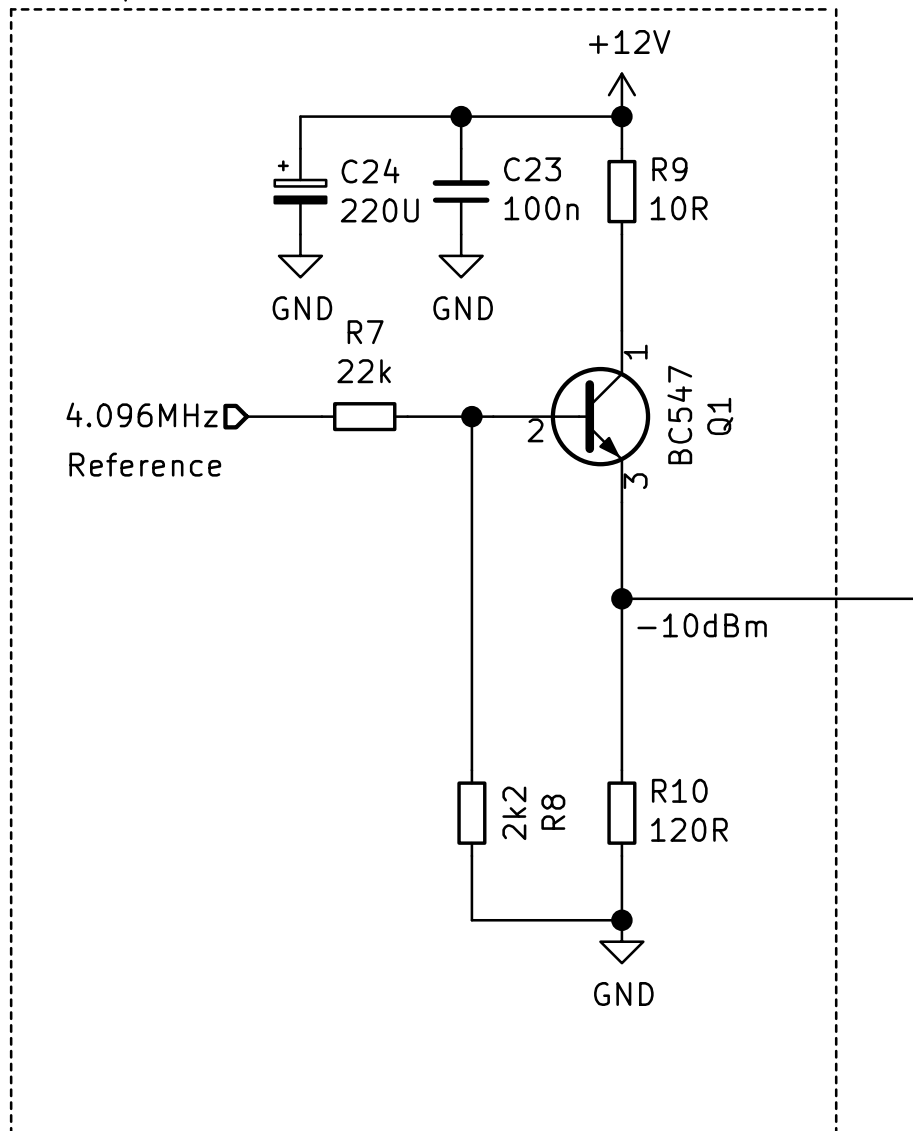


Figure 10: attenuation and impedance matching

Figure 10 shows the attenuator and impedance matching circuit. It attenuates the reference clock from the reference oscillator to about -10dBm with the resistor network R7/R8. The transistor Q1 acts as an active impedance transformer. It is needed to drive the input of the common base amplifier, which has an input impedance of only 50Ω. It is a classic class A amplifier, straight from the book *The art of electronics* second edition, page 912, figure 13.60. In

my design, the amplifier is only biased when the clock is high. This is unusual, but effective as there is no need for a low distortion signal. The clock signal is a square wave anyway! And I am only interested in the low impedance drive capabilities of this amplifier.

4.2 Ripple filter

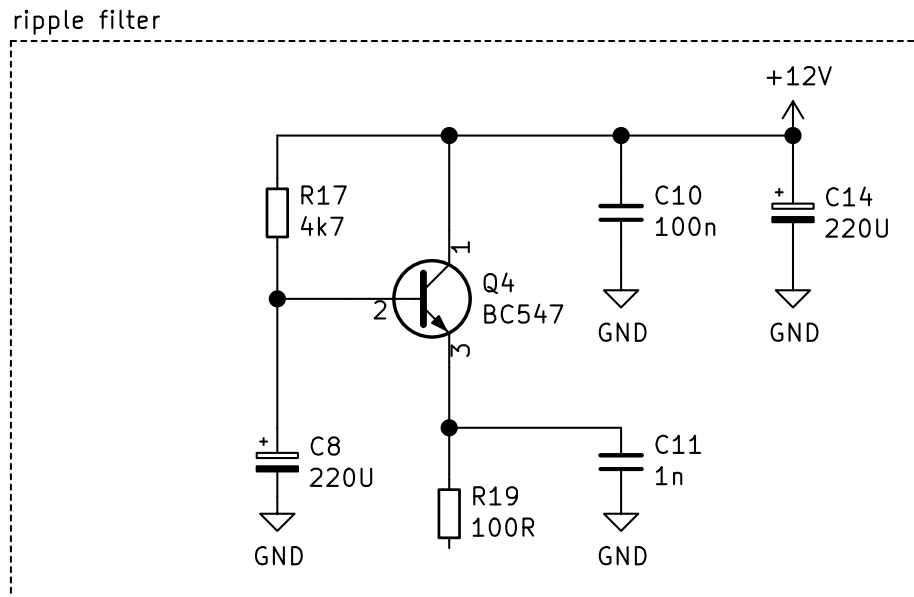


Figure 11: ripple filter

Figure 11 shows the ripple filter. It filters the power supply for the mixer itself. This increases the power supply rejection ratio of the mixer and prevents mixer products from entering the power supply rails. The open end of R19 is connected to the collector side of the mixer.

5 Practical notes

5.1 Build the pcb

Building the printed circuit board is straight forward. The design files are made with KiCad 5.1.8 and scaled PDF files of the printed circuit board are available. The pcb has two layers and I etched it myself. Therefore, there are no plated through vias. All ground connections, as well as some other connections, should be soldered on both sides of the pcb.

A Full schematic

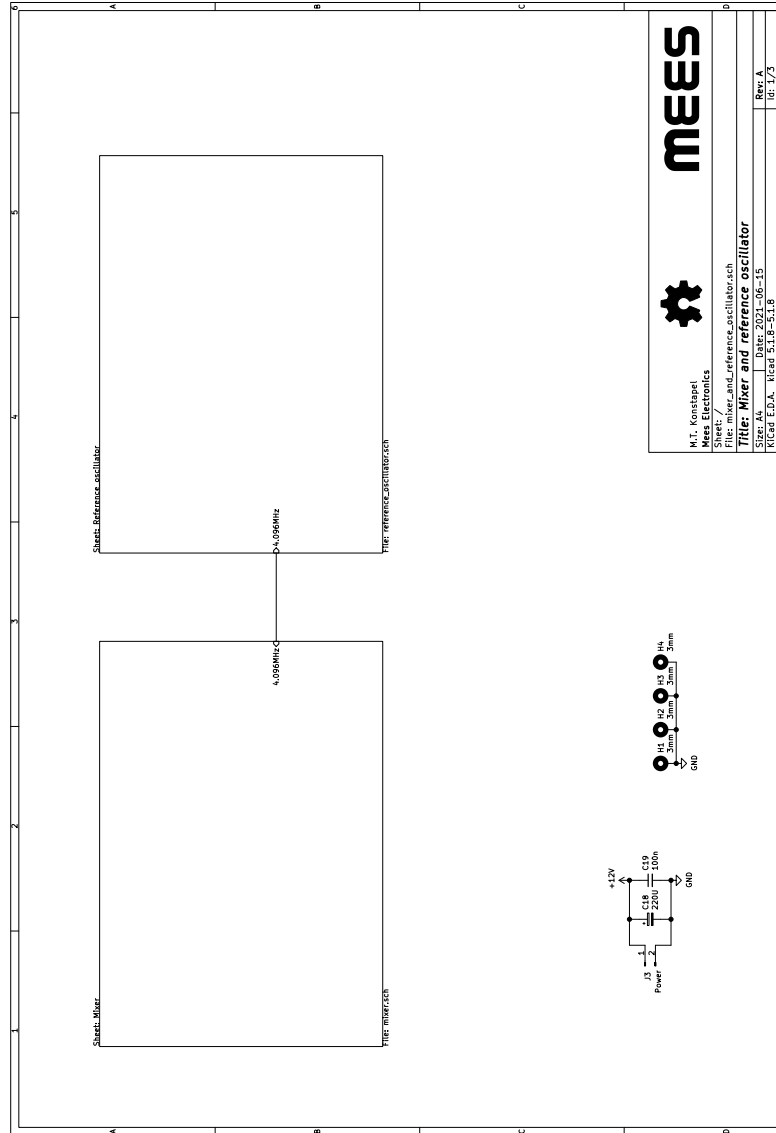


Figure 12: full schematic of mixer and reference oscillator

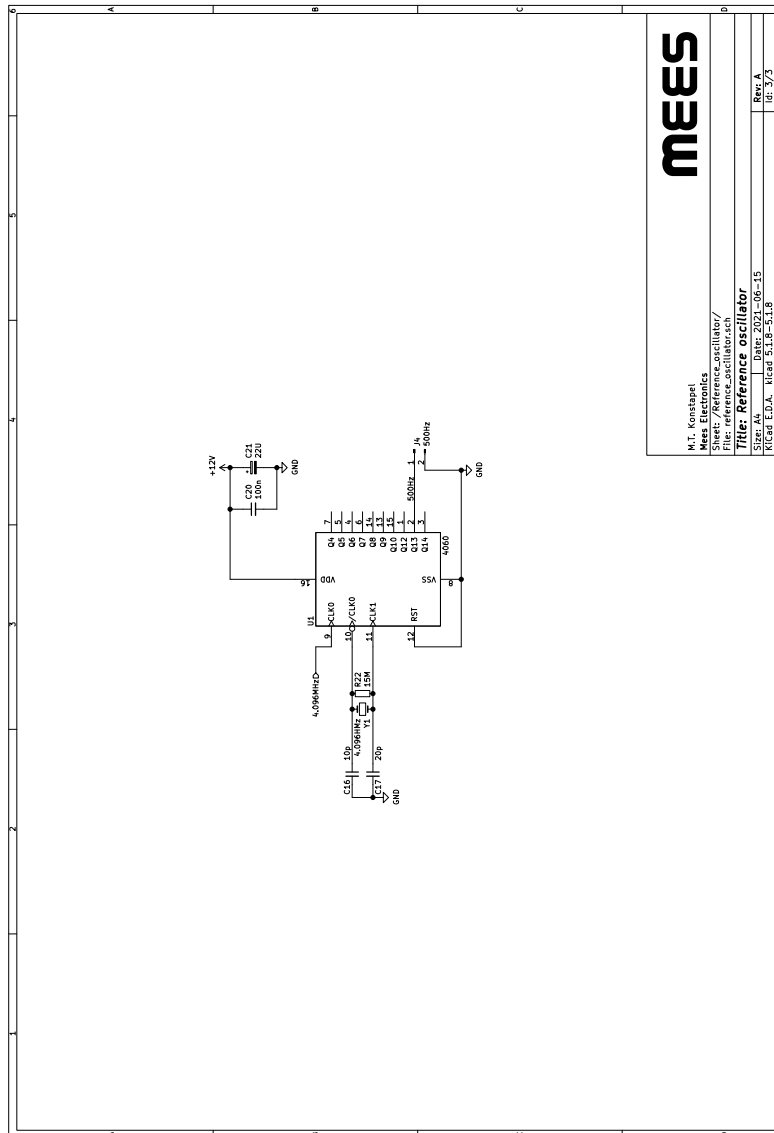
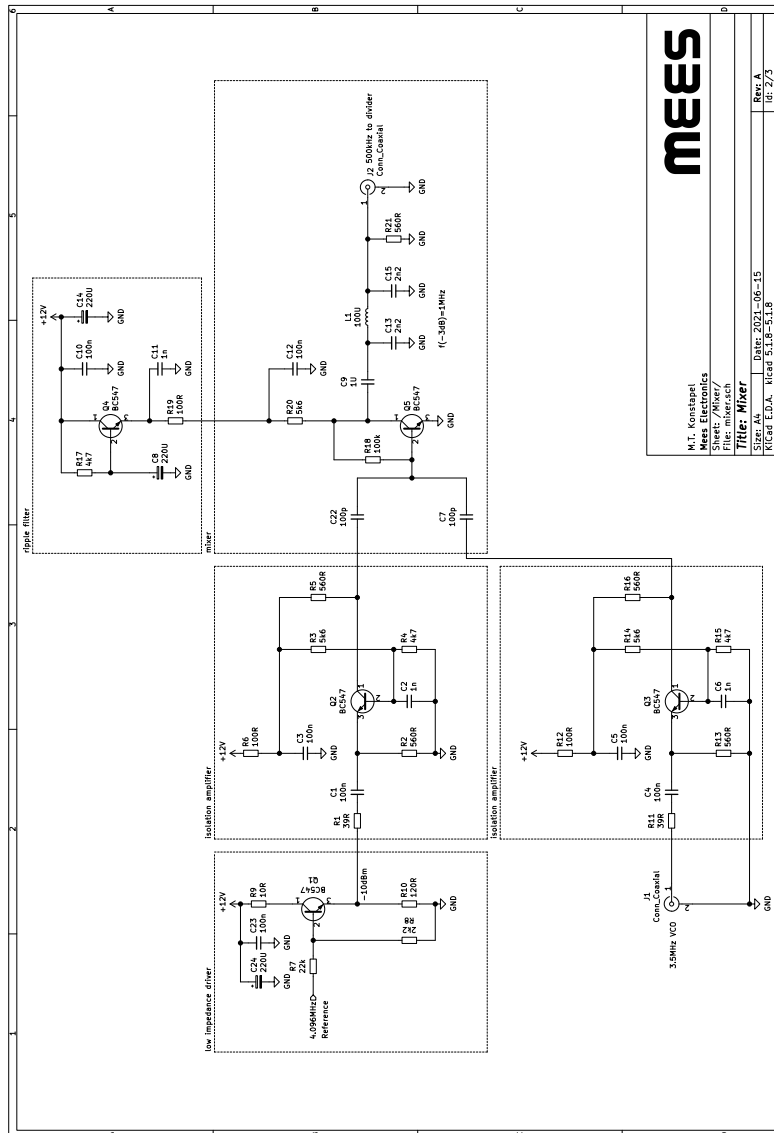


Figure 13: full schematic of reference oscillator



MEES

M.T. Konstapel
 Mees Electronics
 File: mixer.sch
Title: Mixer
 Size: A4 Date: 2021-06-15 Rev: A
 Ricad E.D.A. Ricad 5.1.8-5.1.8 Lib: Z73

Figure 14: full schematic of mixer

B Component placement

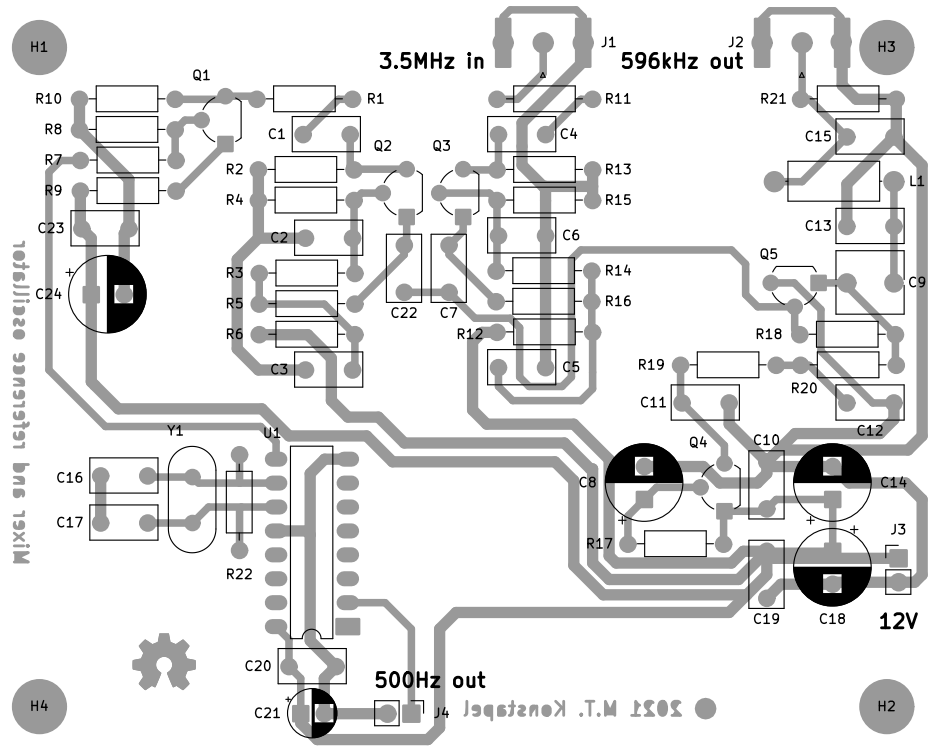


Figure 15: component placement

C Bill of material

#	Reference	Description	Value	Ordering #
1	U1	Binary counter with built-in oscillator	4060	CD4060
9	C19 C12 C10 C5 C4 C3 C1 C23 C20	Capacitor	100n	100n/50V
2	C7 C22	Capacitor	100p	100p/50V
1	C16	Capacitor	10p	10p/50V
3	C2 C6 C11	Capacitor	1n	1n/50V
1	C9	Capacitor	1U	1U/50V
1	C17	Capacitor	20p	20p/50V
2	C13 C15	Capacitor	2n2	2n2/50V
2	J1 J2	Coaxial connector SMA	Conn_Coaxial	do not populate
1	Y1	Crystal	4.096HMz	4.096MHz
4	C8 C14 C18 C24	Electrolitic capacitor	220U	220U/25V
1	C21	Electrolitic capacitor	22U	22U/25V
1	L1	Inductor	100U	100UH
4	H1 H2 H3 H4	Mounting hole	3mm	not a placable part
1	R18	Resistor	100k	100k 1% 0.25W
3	R6 R12 R19	Resistor	100R	100R 1% 0.25W
1	R9	Resistor	10R	10R 1% 0.25W
1	R10	Resistor	120R	120R 1% 0.25W
1	R22	Resistor	15M	15M 1% 0.25W
1	R7	Resistor	22k	22k 1% 0.25W
1	R8	Resistor	2k2	2k2 1% 0.25W
2	R1 R11	Resistor	39R	39R 1% 0.25W
3	R4 R15 R17	Resistor	4k7	4k7 1% 0.25W
5	R2 R5 R13 R16 R21	Resistor	560R	560R 1% 0.25W
3	R3 R14 R20	Resistor	5k6	5k6 1% 0.25W
1	J3 J4	Single row connector	-	2 pin header 2.54mm pitch
5	Q1 Q2 Q3 Q4 Q5	Transistor	BC547	BC547

Figure 16: bill of material

D Open source hardware

All the design files are available on my website: <https://www.meezenest.nl/mees>