Build manual modular transmitter: frequency divider

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Abstract

I obtained my ham radio licence more than twenty years ago and until recently, I had never build a radio transmitter. I will publish a series of articles about the design and build of a modular radio transmitter, using mostly discrete components. The second module I have designed is a frequency divider, which will be part of the PLL.

1 Frequency divider 101

Principle of Phase Locked Loop
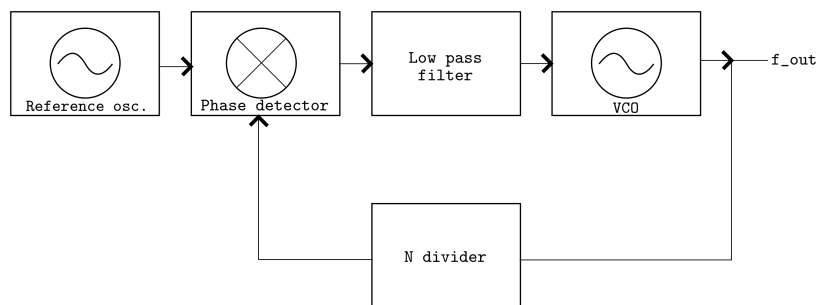
Figure 1: block diagram of a PLL

Figure 1 shows the principle of a PLL. The frequency divider is part of the feedback loop. The PLL I designed, described in the previous article, worked without this divider and was only capable of reproducing the reference oscillator frequency. To synthesize different frequencies, a divider is needed.

Lets assume a reference frequency of 1 kHz and a divider ratio of 250. The output frequency will be 250 kHz, namely 250 times 1 kHz. Or, in other words, the reference frequency is 250 times smaller than the output frequency. When the divider ratio is changed to 251, the output frequency becomes 251 kHz. In this configuration, it is possible to synthesize any frequency with a step size of 1 kHz, by changing the divider ratio N. Because N can only be a whole number, the step size can not be smaller than the reference frequency, which, in this example, is 1 kHz. With a so called fractional-N-divider it s possible to make the step size smaller than the reference frequency. But this is a more complex design and beyond the scope of this article.

2   In-depth analysis

Programmable divider
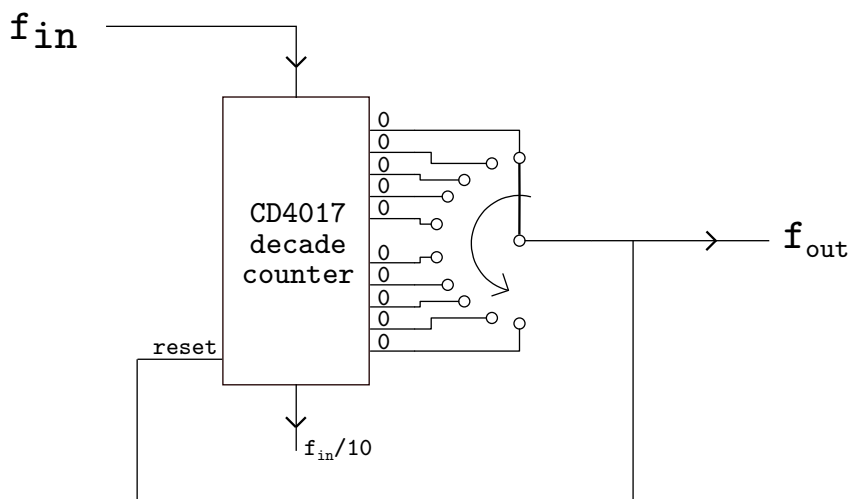
Figure 2: 4017 decade counter

To design a programmable divider, I make use of a 4017 decade counter (see figure 2). As the name suggests it counts from 1 to 10. This chip is designed with frequency division in mind! Lets ignore the switch for now and focus on the ten outputs of the decade counter. A clock signal is connected to the input of the counter. The first output is high. With every new clock pulse the next output switches to high: the clock pulse shifts through the counter. And when it reaches the last output it rolls back to the first output: the cycle repeats. Now, lets look at the whole diagram, including the switch and the feedback to the reset input of the decade counter. Because output zero is selected by the switch, the reset input becomes high and the counter stops counting. When we

select output three of the counter, the reset signal disappears and the counter starts counting again. When it reaches output three, the counter is being reset, but because of that, the reset disappears and the counter starts counting again. The frequency on output f(out) is now three times lower than that of the clock signal. And there you have it: a divider which can be programmed to divide by 0 to 9 by means of a switch. The output on the bottom of the counter can be used to cascade multiple decade counters, thereby increasing the divider ratio.
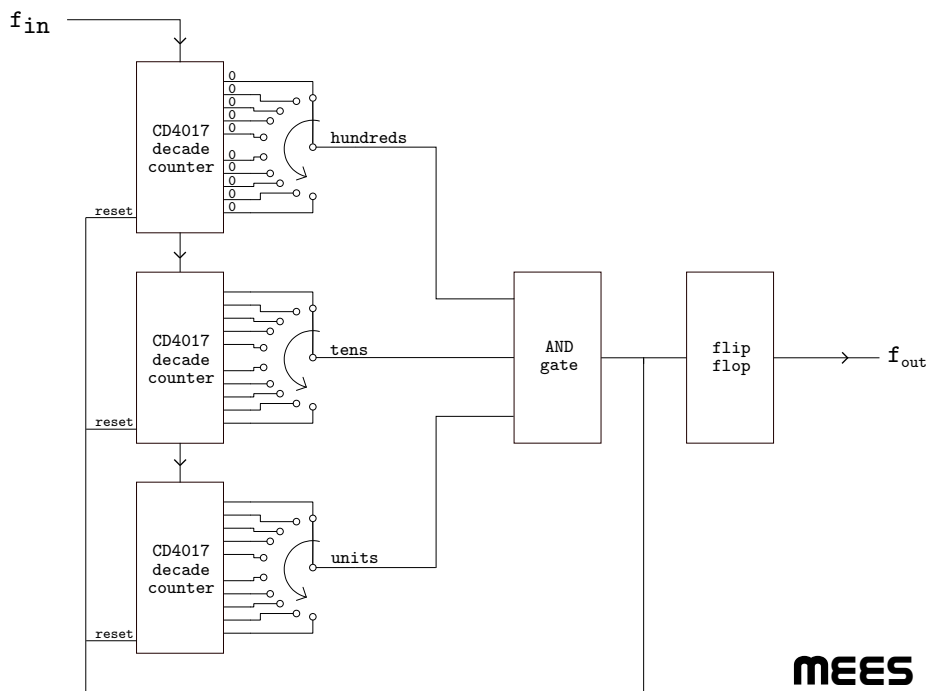
Block diagram divider

Figure 3: Three cascaded decade counters

Which is what you can see in figure 3: three decade counters are placed in cascade. Each counter has its own switch and every switch is connected with an input of the AND-gate. With the switches the divider ratio is set. When the cascaded counters reach this number, the three outputs of the switches are all high at the same time, resetting the counters. Because the reset pulse is very short, it is divided by two with a flip-flop. This reshapes the pulse to a duty-cylce of 50%. At the expense of halving the frequency. Therefore the operating frequency of the PLL must also be halved to preserve the minimum frequency step needed.

3 Design

In figure 4 you can see the decade counter, which is paired with a 16 channel multiplexer. This multiplexer acts as the 10 pole switch. The position of the switch can be set by 4 digital lines: S0...S3. Three sections combined make it
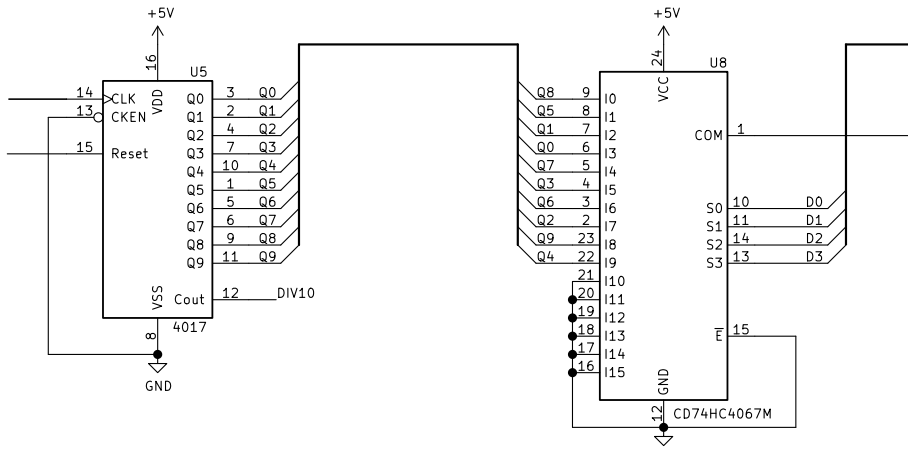
Figure 4: schematic of divider

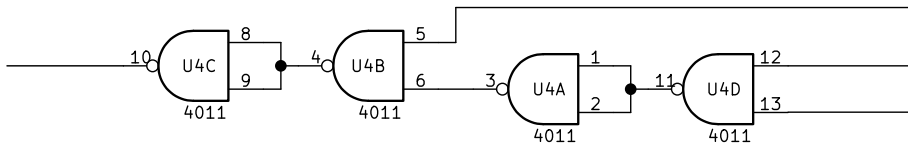possible to set the divider ration between 0 and 999.

Figure 5: schematic of divider

Four NAND gates in figure 5 combine the outputs of the three multiplexer to generate a reset signal, which is also the output signal of the divider.

This signal is fed to a flip-flop (see figure 6), which reshapes the pulse giving it a nice 50% duty-cycle. The circuit above the flip-flop is the clock receiver. This is where the signal from the VCO is connected to. This is the same circuitry as used on the PLL. In the article about the PLL, I explain the working of this part.

To set the multiplexers, I use two shift register (see figure 7). This way it is possible to control the divider via a SPI interface.
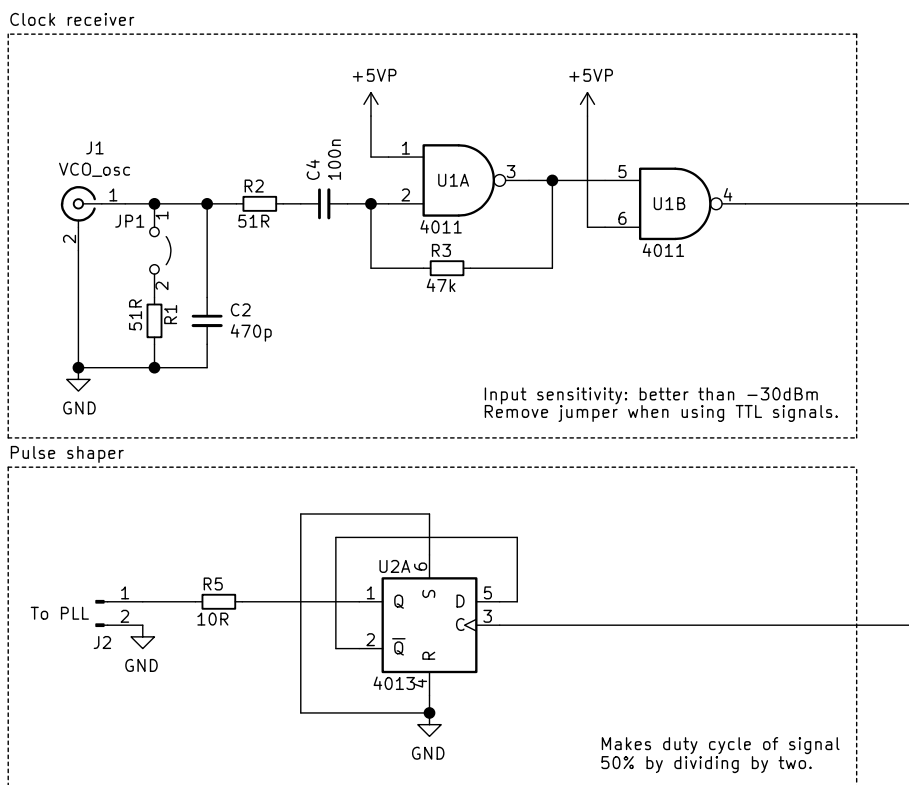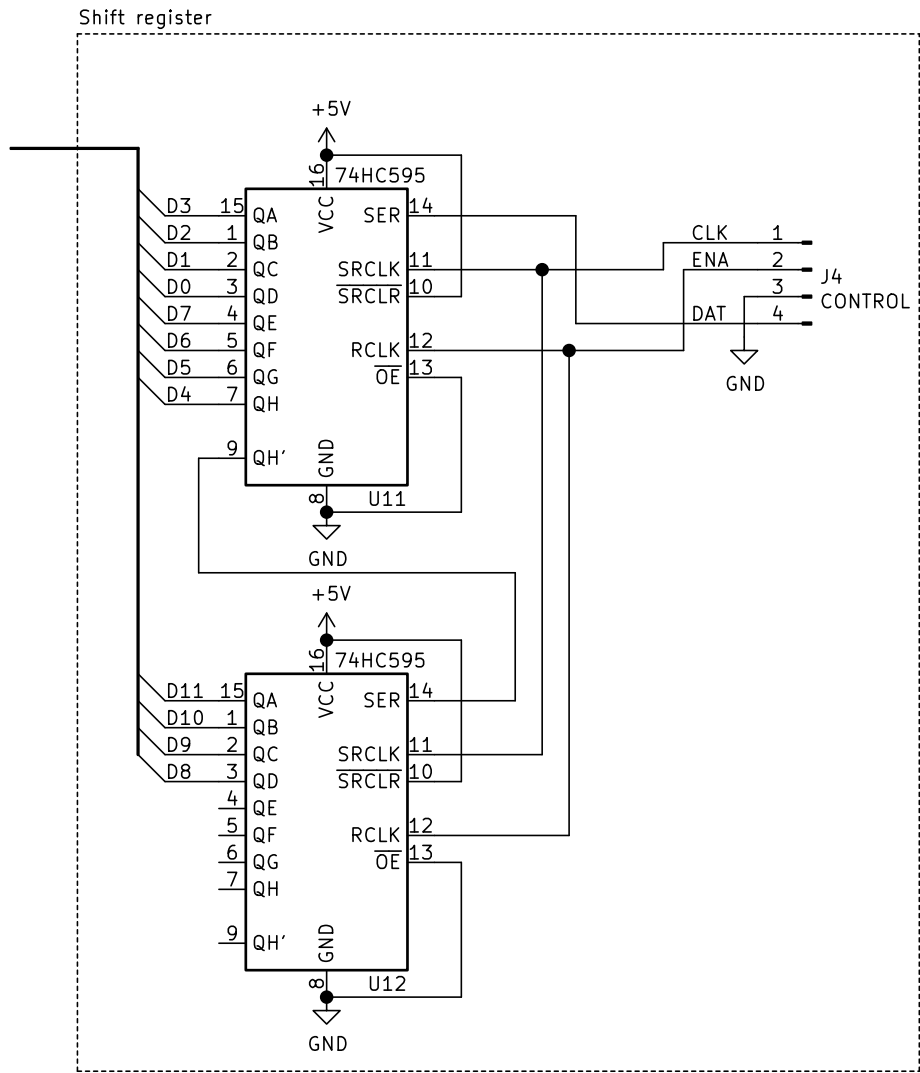
Figure 6: schematic of pulse shaper and clock rceiver

Shift register

+5V

74HC595

D3	15	QA		SER	14
D2	1	QB	VCC 16		
D1	2	QC		SRCLK	11
D0	3	QD		SRCLR	10
D7	4	QE			
D6	5	QF		RCLK	12
D5	6	QG		OE	13
D4	7	QH			
	9	QH′	GND 8		

U11

GND

CLK   1
ENA   2   J4
DAT   4   CONTROL
      3

GND

+5V

74HC595

D11	15	QA		SER	14
D10	1	QB	VCC 16		
D9	2	QC		SRCLK	11
D8	3	QD		SRCLR	10
	4	QE			
	5	QF		RCLK	12
	6	QG		OE	13
	7	QH			
	9	QH′	GND 8		

U12

GND

Figure 7: shift registers
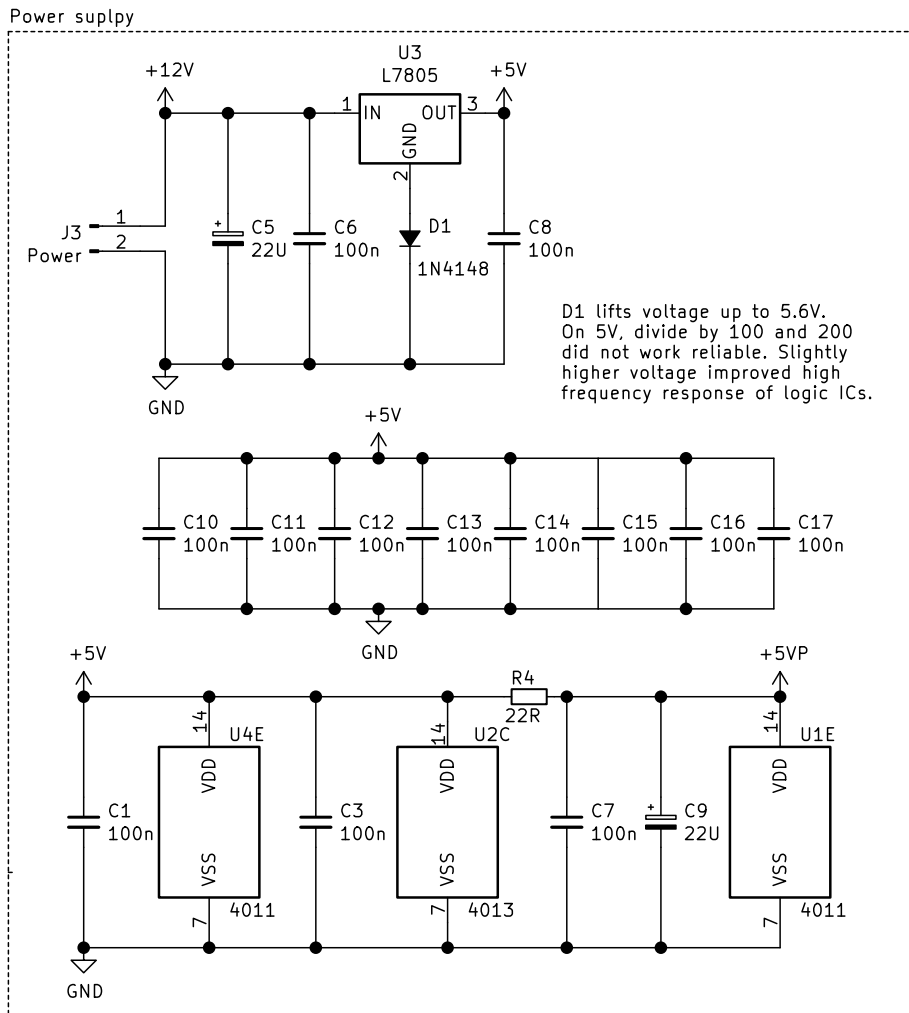
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4 Testing

Power suplpy

Figure 8: power supply

After the first test, I found that the divider was acting up, when set to divider ratios of 100 and 200. When the divider ratio is set to 100 or 200, the reset pulses are very short. To short for some chips to react on it. Luckily, a characteristic of 4000 logic chips is that the maximum working frequency rises when you raise the power supply voltage. Placing a diode in series with the ground lead of the voltage regulator, as shown in figure 8, raised the voltage of the power supply by 0.6 Volts to 5.6 Volts. This was enough to make it all work reliable again. The 74HC595 are very picky about there power supply, but they can operate at up to 7 Volts, so raising the power supply to 5.6 Volts should not cause any issues.

5 Practical notes

5.1 Build the pcb

Building the frequency divider board is straightforward. The design files are made with KiCad 5.1.2 and scaled PDF files of the printed circuit board are available. The pcb has two layers and I etched it myself. Therefore, there are no plated through vias. All ground connections should be soldered on both sides of the pcb, as well al some VCC connections. On the first prototype there were five wire bridges. On later revisions, these are embedded in the top layer.

5.2 Modify the loop filter

In order to get a minimal frequency step of 1 kHz, the pll has to work at 500 Hz (because of the flipflop dividing the signal by two). The frequency response of the loop filter has to change. This can be done by changing the value of C18 from 100nF to 680nF and changing the value of C21 from 4.7nF to 220nF.
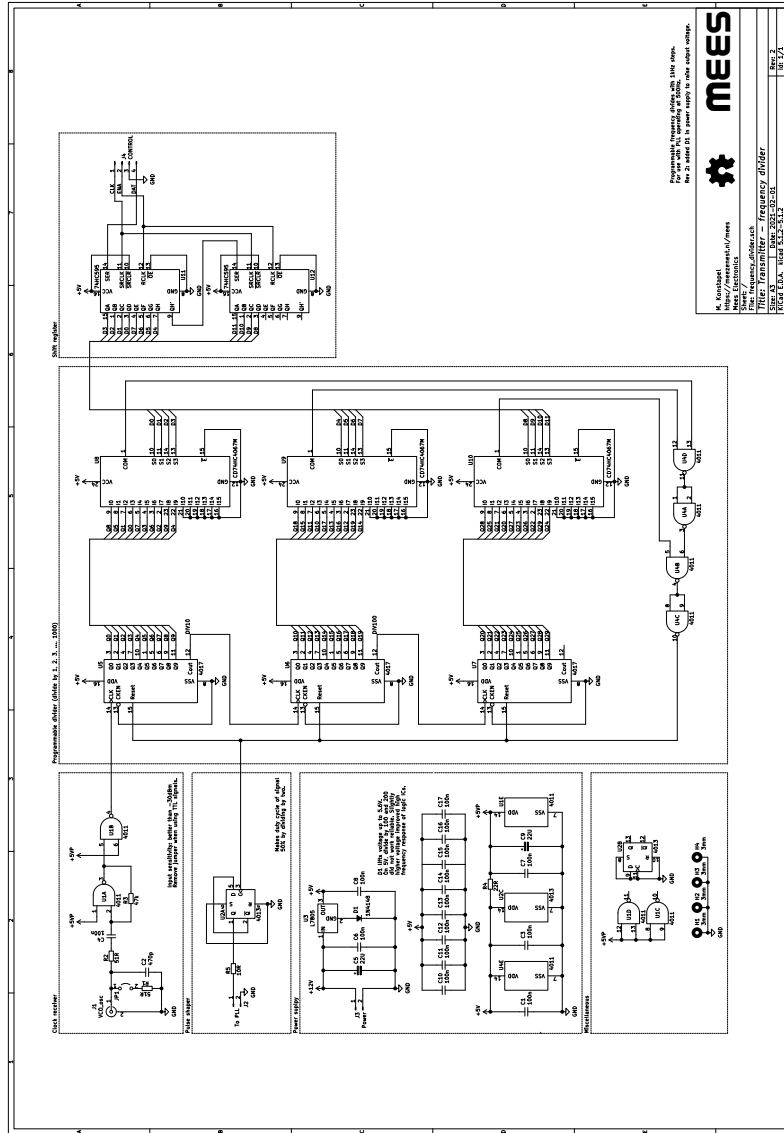
A   Full schematic

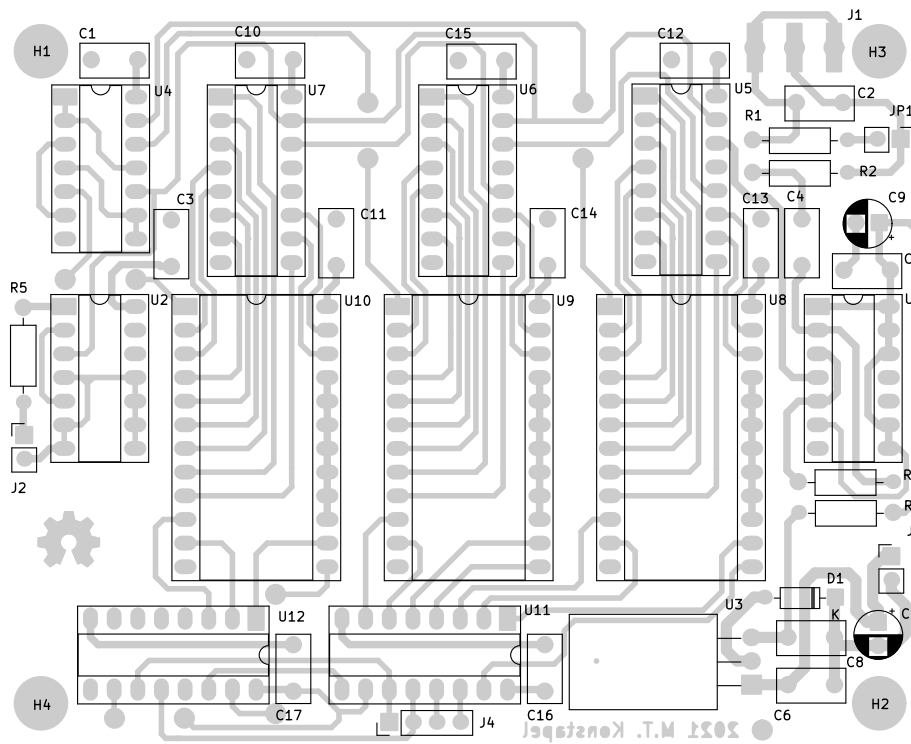Figure 9: full schematic of freqeuncy divider board

B   component placement

Figure 10: component placement

C   Bill of material

#	References	Description	Value	Ordering #
14	C1 C3 C4 C6 C7 C8 C10 C11 C12 C13 C14 C15 C16 C17	Capacitor	100n	100nF 50V 5mm pitch
2	C5 C9	Electrolytic capacitor	22U	22U/50V 2.5mm pitch
1	C2	Capacitor	470p	470pF 50V 5mm pitch
1	D1	Diode	1N4148	1N4148
1	J4	Single row connector	CONTROL	4 pin header 2.54mm pitch
2	J2 J3	Single row connector	To PLL	2 pin header 2.54mm pitch
1	J1	coaxial connector SMA	VCO_osc	SMA edge connector
1	JP1	Single row connector	Jumper_2_Open	2 pin header 2.54mm pitch
1	R5	Resistor	10R	10R 1% 0.25W
1	R4	Resistor	22R	22R 1% 0.25W
1	R3	Resistor	47k	47k 1% 0.25W
2	R1 R2	Resistor	51R	51R 1% 0.25W
2	U1 U4	Quad Nand 2 inputs CMOS	CD4011	CD4011
1	U2	Dual flipflop	CD4013	CD4013
3	U5 U6 U7	Decade counter	CD4017	CD4017
2	U11 U12	Shift register	74HC595	74HC595
3	U8 U9 U10	16 channel mux	CD4067	CD4067
1	U3	5 volt regulator	LM7805	LM7805

Figure 11: bill of material

D   Open source hardware

All the design files are available on my website: https://www.meezenest.nl/mees